Design and Analysis of 4:2 Approximate Compressors using GDI Technique for Multiplication

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Abstract – Multiplication is a fundamental operation in most of the digital logic circuits. Multipliers occupy large area, exhibit long latency and consume considerable power. The design of multipliers is a challenge for VLSI system designers. 4:2 approximate compressors are designed in GDI technology. Designed 4:2 approximate GDI compressors are used in Dadda multiplier. These compressors designs are verified and synthesized using Tanner T-Spice tools at 32nm technology. The results show that the approximate GDI compressors designs accomplish significant reduction in power dissipation, delay, transistor count and power delay product compared to approximate CMOS compressors designs.

Index Terms – GDI (gate diffusion input), CMOS (complementary metal oxide semiconductor).

1. INTRODUCTION

In most of the applications, multipliers have been the critical and obligatory component dictating the overall circuit performance when constrained by power consumption and computation speed. At the circuit design level, considerable potential for optimizing the power-delay product of the multiplier exists by voltage scaling and through the use of contemporary and new CMOS logic styles for the implementation of its embraced combinational circuits [1][2]. A fast array or tree multiplier is typically composed of three sub circuits: a Booth encoder for the generation of a reduced number of partial products; a carry save structured accumulator for a further reduction of the partial products' matrix to only the addition of two operands; and a fast carry propagation adder (CPA) for the computation of the final binary result from its stored carry representation. Among these sub circuits, the second stage of partial product accumulation, often referred to as the carry save adder (CSA) tree [3], occupies a high fraction of silicon area, contributes most to the overall delay, and consumes significant power. Therefore, speeding up the CSA circuit and lowering its power dissipation are crucial to sustain the performance of the multiplier to stay competitive. Early designs of CSA tree used the Dadda's column compression technique with the 3-2 counters, or equivalently the full adders to reduce the partial product matrix. To lower the latency of the partial product accumulation stage, 4-2 compressors have been widely employed nowadays for high speed multipliers. Owing to its regular interconnection, the 4-2 compressor is ideal for the construction of regularly structured Wallace tree with low complexity. Several 4-2 compressor circuits have been designed for low-power applications. Some of these are able to operate at low supply voltages but require excessive number of transistors due to their complementary CMOS structures, others use smaller number of transistors but fail to function at ultralow voltages, or lack the driving capability to drive the next level of sub circuits.

The insertion of additional buffers for every output ports to provide the output drive increases the switching activities and hence the power dissipation. Most of the research on high-input compressors focuses on the optimization of circuit structure for high speed applications at standard supply voltages. With trends in VLSI toward deep-sub micrometer technology, circuits operating reliably at sub-1 V will soon become a reality [4]. This is because the materials used to form the transistors cannot withstand an electric field of unlimited strength, and as transistors get smaller, the field strength increases if the supply voltage is held constant. Since supply voltage has a quadratic contribution to the power dissipation, lowering the supply voltage is also a lucid means of reducing power consumption.

However, the major problem with reducing the supply voltage is that the speed of the circuits is also degraded. Therefore, there is a strong impetus to renew the full custom arithmetic cells to achieve high power efficiency for VLSI circuits operating at ultralow supply voltages. In this paper, we explore new design methodologies for low power 4-2 compressor circuits using GDI technology.

2. EXISTING COMPRESSORS

The 4:2 Compressor has 5 inputs X1, X2, X3, X4 and C_{in} to generate 3 outputs Sum, Carry and C_{out} as shown in Figure 4 (a) .The 4 inputs X1, X2, X3, X4 and the output Sum have the same weight [5][6]. The input C_{in} is the output from a previous lower significant compressor and the output C_{out} is for the compressor in the next significant stage. The conventional approach to implement 4:2 compressors is with 2 full adders connected serially as shown in Figure 4(b)

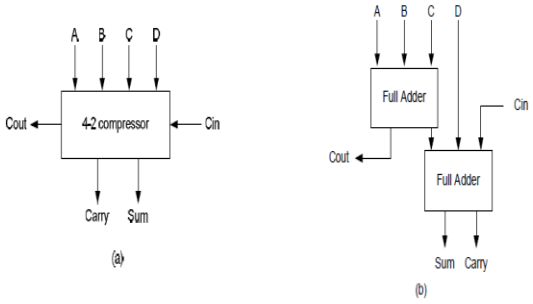


Figure 1 (a) 4-2 adder compressor. (b) 4-2 adder compressor implemented with full adders.

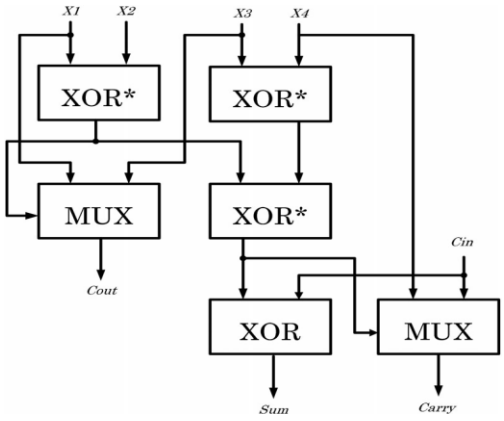
X1+X2+X3+X4+CIN=SUM+2(CARRY+COUT) (1)

A.APPROXIMATE 4:2 COMPRESSOR

Table-1 Approximate 4:2 compressor

C_{IN}	X_4	X_3	X_2	X_1	C_{OUT}	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

Approximate compressor are designed - one with C_{in} and other without C_{out}. Intuitively to design an approximate 4:2 compressor, it is possible to substitute the exact full-adder cells in Figure 3.5 by an approximate full-adder cell. However, this is not very efficient, because it produces at least 17 incorrect results out of 32 possible outputs, i.e. the error rate of this inexact compressor is more than 53%. Two different designs are designed next to reduce the error rate; these designs offer significant performance improvement compared to an exact compressor with respect to delay, number of transistors and power consumption.



$$c_{\text{out}} = (x_1 \oplus x_2) \cdot x_3 + x_1 \cdot x_2 = (x_1 \oplus x_2) \cdot x_3 + \overline{(x_1 \oplus x_2)} \cdot x_1$$

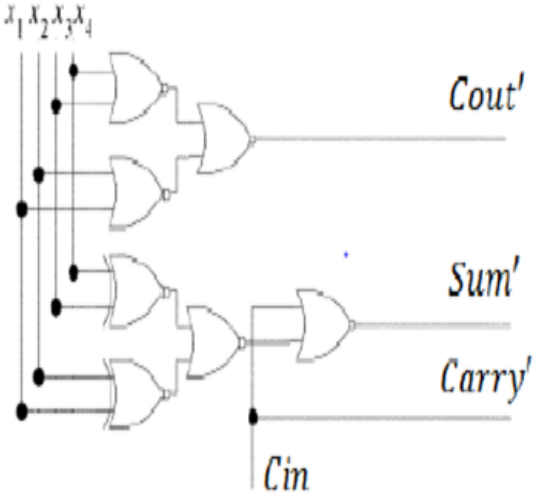
$$s = x_1 \oplus x_2 \oplus x_3$$

$$\text{sum} = s \oplus x_4 \oplus c_{\text{in}} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_{\text{in}}$$

$$\text{carry} = (s \oplus x_4) \cdot c_{\text{in}} + s \cdot x_4 = (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot c_{\text{in}} + \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)} \cdot x_4.$$

B. APPROXIMATE 4:2 COMPRESSOR WITH Cin

As shown in Table 2, the design has 12 incorrect outputs out of 32 outputs (thus yielding an error rate of 37.5%). This is less than the error rate using the best approximate GDI full-adder cell of exact compressor.



$$\text{Carry'} = \text{Cin}$$

$$Sum' = \overline{Cin}(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$Cout' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

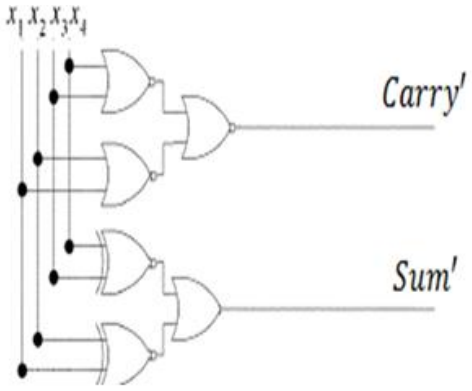
Table-2 Approximate compressor with C_{in}

C_{IN}	X_4	X_3	X_2	X_1	C_{OUT}	Carry'	Sum	Difference
0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	1	0
0	0	0	1	1	0	0	1	-1
0	0	1	0	0	0	0	1	0
0	0	1	0	1	1	0	0	0
0	0	1	1	0	1	0	0	0
0	0	1	1	1	1	0	1	0
0	1	0	0	0	0	0	1	0
0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	0
0	1	0	1	1	1	0	1	0
0	1	1	0	0	0	0	1	-1
0	1	1	0	1	1	0	1	0
0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	0	1	-1
1	0	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	0	-1
1	0	1	0	0	0	1	0	0
1	0	1	0	1	1	1	0	1
1	0	1	1	0	1	1	0	1
1	0	1	1	1	1	1	0	0
1	1	0	0	0	0	1	0	0
1	1	0	0	1	1	1	0	1
1	1	0	1	0	1	1	0	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	0	1	0	-1
1	1	1	0	1	1	1	0	0
1	1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0	-1

C. APPROXIMATE 4:2 COMPRESSOR

WITHOUT Cin

This design has 4 incorrect outputs out of 16 outputs, so its error rate is now reduced to 25%. This is a very positive feature, because it shows that on a probabilistic basis, the imprecision of the design is smaller than the other available schemes.



$$Sum' = (\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$Carry' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

Table-3 Approximate compressor without cin

X_4	X_3	X_2	X_1	Carry'	Sum'	Difference
0	0	0	0	0	1	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	-1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	-1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	-1

3. GDI TECHNIQUE

In this paper, new design methodologies for low power 4-2 compressor circuits using GDI technology is implemented. By investigating the performances of several fast 4-2 GDI compressor architectures and their underlining building modules, a new composite exclusive OR (XOR) and exclusive NOR (XNOR) [XOR–XNOR] cell is designed. The GDI 4-2 compressors constructed around the XOR–XNOR cell exhibit superior power efficiency comparing to CMOS 4:2 compressor. A new fast 4-2 GDI compressor architecture is designed, together with a new circuit for its carry generator module. This new architecture performs well with almost any configuration of logic styles and its overall performance is the best among the known GDI 4-2 compressor architectures under a realistic simulation environment that truly reflects its actual operability in a tree-structured multiplier [7].

In recent trends the digital designs concentrate more on high speed, high throughput, small silicon area and low power consumption of the digital circuit. Gate Diffusion Input (GDI) based full adder plays an eminent role in low power applications [8]. GDI cell method is based on the use of a simple cell. In general, a simple GDI cell consists of three inputs as shown in Figure

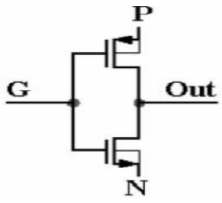


Fig::Basic GDI Cell

i) G – Common gate input to both NMOS and PMOS

ii) P – Input to either source or drain of PMOS

iii) N – Input to either source or drain of NMOS

When the bulk of both NMOS and PMOS get connected, then the design resembles that of a CMOS inverter.

Multiplication

The impact of using the GDI compressors for multiplication is investigated. A fast (exact) multiplier is usually composed of three parts (or modules)[9].

• Partial product generation.

• A Carry Save Adder (CSA) tree to reduce the partial products' matrix to an addition of only two operands [10]

• A Carry Propagation Adder (CPA) for the final computation of the binary result.

In the design of a multiplier, the second module plays a pivotal role in terms of delay, power consumption and circuit complexity. GDI Compressors have been widely used to speed up the CSA tree and decrease its power dissipation, so to achieve fast and low-power operation. The use of approximate GDI compressors in the CSA tree of a multiplier results in an approximate GDI multiplier.

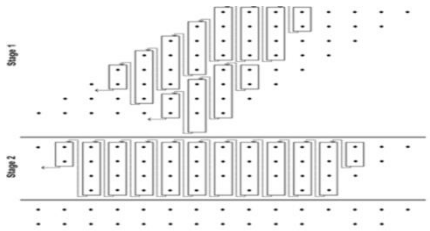


Fig 5 Dadda Multiplier using approximate GDI compressor with cin

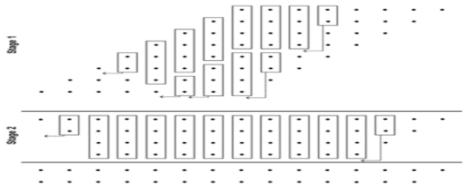


Fig 6 Dadda Multiplier using approximate GDI compressor without cin

4. SIMULATIONS RESULTS

The GDI compressors are implemented and simulated using Tanner tool at 32nm technology The simulation waveform of exact GDI compressor is shown in figure 8. For the input 11111, the output sum=1,cout=1 and carry=1 are obtained. The power, delay values obtained are 1.964*10^-6 (watt) and 4.919*10^-8 (sec).The power and delay values obtained are less when compared to the Exact compressor using CMOS design.

Exact GDI compressor

Figure 8 Exact GDI compressor waveform

Approximate GDI Compressor

Schematic diagram of approximate GDI compressor consists of GDI XOR-XNOR, GDI MUX, five inputs namely X1,X2,X3,X4,Cin and produce outputs Sum, Carry and C_{out}. The simulation waveform of approximate GDI compressor is shown in figure 9. The circuit is simulated in Tanner EDA at the operating voltage of 1v. For the input 11111 the output sum=1 and carry=1 is obtained. The power, delay values obtained are 1.731*10^-6 (watt) and 2.066*10^-8 (sec). By using the approximate design the power and delay values are reduced when compared to the exact GDI compressor and Approximate CMOS compressor design.

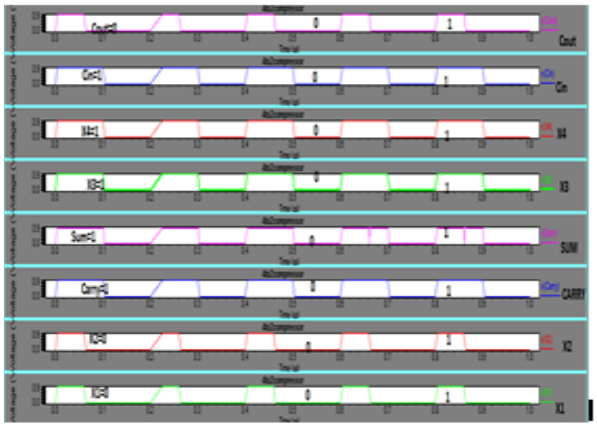


Figure 9 Approximate GDI compressor waveform

Approximate GDI Compressor with Cin

Using approximate GDI compressor with C_{in} design it produces 12 incorrect results out of 32 outputs. The error rate is reduced when compared with the approximate GDI compressor design. Schematic Diagram of approximate GDI

compressor with C_{in} consists of GDI NOR, GDI X-NOR, GDI OR gate designs, five inputs namely X1, X2, X3, X4, Cin and produce outputs Sum, Carry and C_{out}. For the different combinations of the inputs the outputs sum, carry and C_{out} are simulated using tanner tool, at 32nm technology shown in figure 10. The power, delay values obtained are 8.80*10^-6 (watt) and 1.709*10^-11 (sec). By using the approximate GDI compressor with C_{in} design the power and delay values are reduced when compared to the approximate GDI compressor and approximate CMOS compressor with C_{in} design.

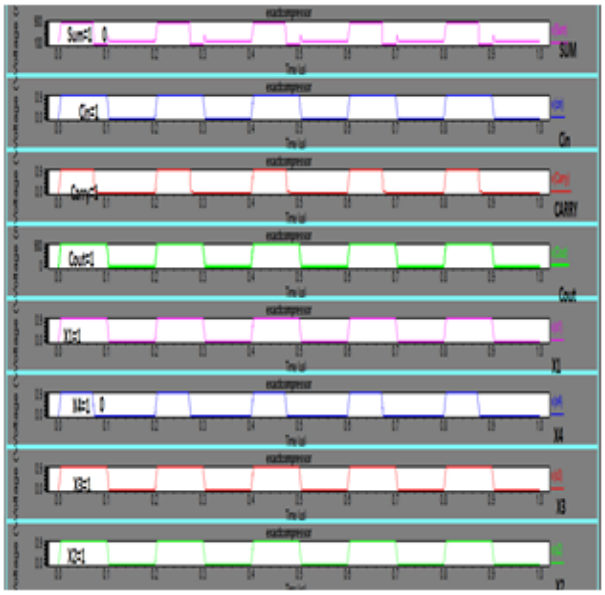


Figure 10 Approximate GDI compressor with C_{in} waveform

Approximate GDI Compressor without Cin

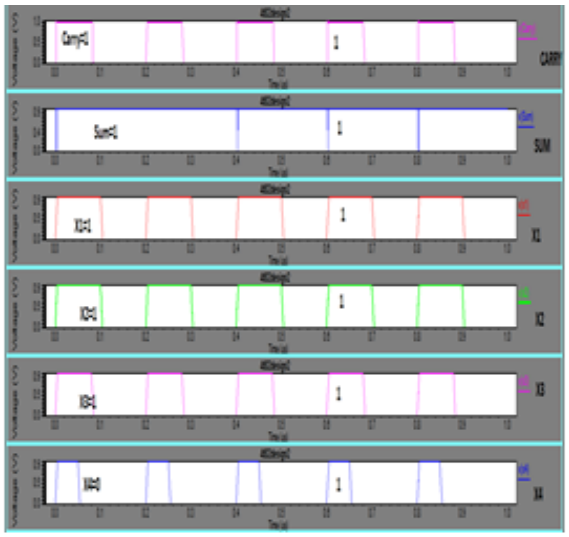


Figure 11 Approximate GDI compressor with C_{in} waveform

By using approximate GDI compressor without C_{in} design it produces 4 incorrect results out of 16 outputs. The error rate is reduced when compared with the approximate GDI compressor with C_{in} design. Schematic Diagram of approximate GDI compressor without C_{in} consists of GDI NOR, GDI XNOR, GDI OR gates, four inputs namely X1,X2,X3,X4 and produce the outputs sum, carry. For the input 1111 the output sum=1 and carry=1 is obtained and shown in figure 11. The power, delay values obtained are 2.148*10^-4 (watt) and 8.160*10^-11 (sec). By using the approximate GDI compressor without C_{in} design the power and delay values are reduced when compared to the approximate GDI compressor with C_{in} and approximate CMOS compressor without C_{in} design (table-6).

Dadda Multiplier

The simulation waveform of Dadda multiplier of approximate GDI compressor without C_{in} is shown in figure 12. The circuit is simulated in Tanner EDA at the operating voltage of 1v. For the input x=01110111, input y=01001111 the output 001110001011101 is obtained.

The power, delay values obtained are 1.4619*10^-3 (watt) and 4.84*10^-8 (sec). By using this design the power and delay values obtained are less when compared with the values of dadda multiplier of approximate GDI compressor with C_{in} and dadda multiplier of approximate compressor with C_{in} using CMOS design (table -7).

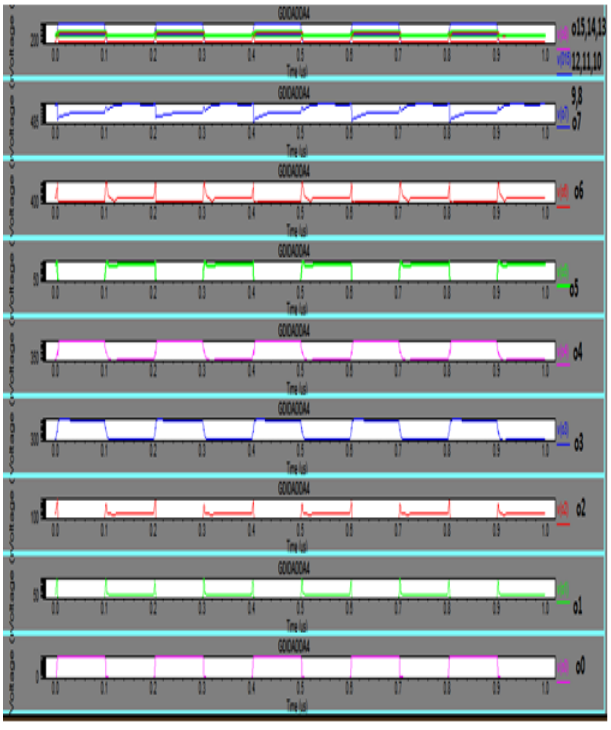


Figure 11 Dadda multiplier of approximate GDI compressor waveform without C_{in}

Table -4 Comparison of 4:2 Compressors

CIRCUIT NAME	POWER (WATT)	DELAY (SEC)	PDP (JOULES)
Exact compressor	2.799E-6	4.954E-8	1..386E-13
Approximate compressor	1.729E-6	2.509E-8	4.339E-14
Approximate compressor with C_{in}	1.171E-6	1.431E-10	1.675E-16
Approximate compressor without C_{in}	1.131E-6	1.792E-10	2.028E-16
Dadda multiplier using exact compressor with C_{in}	2.027E-3	4.841E-8	9.814E-11
Dadda multiplier using exact compressor without C_{in}	1.814E-3	4.841E-8	8.782E-11
Dadda multiplier using approximate compressor with C_{in}	1.563E-3	4.841E-8	7.567E-11
Dadda multiplier using approximate compressor without C_{in}	1.652E-3	4.841E-8	8.000E-11

Table -5 Comparison of 4:2 compressors using GDI technique

CIRCUIT NAME	POWER (WATT)	DELAY (SEC)	PDP (JOULES)
Exact compressor	1.964E-6	4.919E-8	9.6661E-14
Approximate compressor	1.731E-6	2.066E-8	3.576E-14
Approximate compressor with C_{in}	8.807E-6	1.709E-11	1.505E-16
Approximate compressor without C_{in}	2.148E-6	8.160E-11	1.748E-16
Dadda multiplier using exact compressor with C_{in}	2.024E-3	4.50E-8	9.128E-11
Dadda multiplier using exact compressor without C_{in}	1.95E-3	4.182E-8	8.154E-11
Dadda multiplier using approximate compressor with C_{in}	1.514E-3	4.021E-8	6.087E-11
Dadda multiplier using approximate compressor without C_{in}	1.461E-3	4.841E-8	7.075E-11

The comparison of power, delay and power delay product of different designs of 4:2 GDI compressors are shown in table 5. The power, delay and PDP values of GDI compressors are decreased when compared to CMOS compressors design.

Table-6 Comparison of Power delay products of 4:2 compressors and Percentage improvement.

CIRCUIT NAME	PDP (JOULES)	PDP (JOULES)	(% improvement in PDP)
Exact compressor	1..386E-13	9.6661E-14	30
Approximate compressor	4.339E-14	3.576E-14	17
Approximate compressor with C_{in}	1.675E-16	1.505E-16	10
Approximate compressor without C_{in}	2.028E-16	1.748E-16	7.9
Dadda multiplier using exact compressor with C_{in}	9.814E-11	9.128E-11	20
Dadda multiplier using exact compressor without C_{in}	8.782E-11	8.154E-11	11
Dadda multiplier using approximate compressor with C_{in}	7.567E-11	6.087E-11	7.1
Dadda multiplier using approximate compressor without C_{in}	8.000E-11	7.075E-11	6.8

Comparison of Power delay products of 4:2 Approximate compressors and their Percentage improvement in Power delay product is tabulated in table 6. The PDP (%) is also calculated. The PDP values of GDI compressors are decreased when compared to CMOS compressors design

5. CONCLUSION

By an approximate GDI compressor, multipliers can be designed for inexact computing. These multipliers offer significant advantages in terms of both circuit-level and error figures of merit. These designs may also be useful in other arithmetic circuits for applications in which inexact computing can be used. The approximate GDI compressors show a significant reduction in transistor count, power consumption, delay and PDP compared with 4:2 CMOS compressor designs.

In terms of the PDP, the Exact GDI compressor has 30% improvement than the exact CMOS compressor design, The approximate GDI compressor has 17% improvement than the approximate CMOS compressor design, The approximate GDI compressor with C_{in} has 10% improvement than the approximate CMOS compressor with C_{in} design, The approximate GDI compressor without C_{in} has 7.9% improvement than the approximate CMOS compressor without C_{in} design.

Two different GDI approximate schemes have been designed to investigate the performance of the approximate GDI compressors for inexact multiplication. The approximate GDI compressors have been utilized in the reduction module of a Dadda multiplier.

The following conclusion

ns can be drawn from the simulation results in terms of their Power delay product.

Dadda multiplier of exact GDI compressor with C_{in} has 20% improvement than the Dadda multiplier of exact CMOS compressor with C_{in} design, Dadda multiplier of exact GDI compressor without C_{in} has 11% improvement than the Dadda multiplier of exact CMOS compressor without C_{in} design, Dadda multiplier of approximate GDI compressor with C_{in} has 7.1% improvement than the Dadda multiplier of approximate CMOS compressor with C_{in} design, Dadda multiplier of approximate GDI compressor without C_{in} has 6.8% improvement than the Dadda multiplier of approximate CMOS compressor without C_{in} design.

Power delay product is low compared to other designs which determine the figure of merit. So the figure of merit of GDI circuits is improved and they are power efficient. Thus GDI compressors can be used in applications where low power and less area is required. In the future, 16-bit, 32-bit multiplier using GDI based compressors can be optimized.

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